We claim:

1. A method of forming a memory device comprising:

preparing a substrate having predefined characteristics;

forming a first layer set on the substrate, including:

building a first forming layer, having first form segments, on the substrate;

building placeholder sidewalls on the first form segments;

building a second forming layer, having second form segments, on the substrate between the placeholder sidewalls;

removing the placeholder sidewalls forming vacated areas; and

building active devices in the vacated areas.

2. The method of claim 1 wherein said building placeholder sidewalls includes depositing a layer of nitride to a thickness of between about one nm and 100 nm.

3. The method of claim 1 wherein said building a first forming layer includes forming a layer of silicon oxide to a thickness of between about 100 nm to 1000 nm.

4. The method of claim 1 wherein said building a second forming layer includes forming a layer of silicon oxide to a thickness of between about 100 nm to 1000 nm.

5. The method of claim 1 wherein said forming vacated areas includes forming plural, substantially parallel vacated areas in the first layer set.

6. The method of claim 5 which includes forming a second layer set, having the same components of the first layer set, having plural vacated areas therein on the first layer set, wherein the vacated areas of the second layer set are substantially normal to the vacated areas of the first layer set, and wherein active device are built at the intersection of the vacated areas in the first layer set and the vacated areas in the second layer set.

7. The method of claim 6 which includes forming word lines in the vacated areas of the first layer set.

8. The method of claim 1 which includes forming a doped oxide layer on the substrate before building the first forming layer.

9. The method of claim 8 wherein said forming a doped oxide layer includes forming a borosilicated glass layer on the substrate.

10. A method of forming a memory device comprising:

preparing a substrate having predefined characteristics;

building first form segments on the substrate to form one wall of regions which will be used for active device construction, word lines, bit lines and ground lines;

depositing placeholder sidewalls to a thickness of between about one nm and 100 nm on the first form segments;

building second form segments on the substrate between the placeholder sidewalls to form a spaced apart other wall of regions for active device construction, word lines, bit lines and ground lines;

removing the placeholder sidewalls forming vacated regions; and

building active devices, word lines, bit lines and ground lines in the vacated regions.

11. The method of claim 10 wherein said building the first form segments includes forming a layer of silicon oxide to a thickness of between about 100 nm to 1000 nm.

12. The method of claim 10 wherein said building the first form segments includes forming a layer of silicon oxide to a thickness of between about 100 nm to 1000 nm.

13. The method of claim 10 wherein said forming vacated regions includes forming plural, substantially parallel vacated areas.

14. The method of claim 10 which includes forming a doped oxide layer on the substrate before building the first forming layer.

15. The method of claim 14 wherein said forming a doped oxide layer includes forming a borosilicated glass layer on the substrate.

16. A method of forming a memory device comprising:

preparing a silicon substrate;

forming a first layer set on the substrate, comprising:

depositing a first oxide layer and etching the first oxide layer to form first oxide segments;

depositing a first nitride layer to a thickness of between about one nm and 100 nm and etching the nitride layer to form nitride sidewalls about the oxide segments;

depositing a second oxide layer to form second oxide segments between the nitride sidewalls of the first oxide segments;

forming contact area in the first and second oxide layers, including forming bit contact areas and ground contact areas;

etching the nitride sidewalls to form microtrenches which extend between bit contact areas and ground contact areas;

depositing a layer of epitaxial silicon; and

depositing a layer of PSG;

forming a second layer set, comprising:

depositing a third oxide layer and etching the third oxide layer to form third oxide segments;

depositing a second nitride layer to a thickness of between about one nm and 100 nm and etching the nitride layer to form nitride sidewalls about the third oxide segments which sidewalls are substantially normal to the nitride sidewalls formed by the first nitride layer;

depositing a fourth oxide layer to form fourth oxide segments between the

nitride sidewalls of the third oxide segments;

etching the second nitride sidewalls to form microtrenches;

selectively etching the layers to the level of the PSG layer to form trenches;

depositing a tunnel oxide layer in the trenches;

depositing a first polysilicon layer and selectively etching the first polysilicon layer to the level of the PSG;

depositing a polysilicon oxide layer;

depositing a second polysilicon layer and plasma etching the second polysilicon layer to form word lines; and

implanting impurities, annealing, and metallizing the device.